

1     1.     A method for synthesizing a clock distribution circuit within an integrated circuit  
2           device, said device comprised of a plurality of functional circuits and placed on a  
3           substrate, said method comprising the steps of:

4                 allocating at least one delaying circuit within each of said functional  
5                 circuits;

6                 fabricating an intra-functional clock distribution network within each of the  
7                 functional circuits;

8                 fabricating an inter-functional clock distribution network between each of  
9                 the functional circuits;

10                determining a clock skew for the inter-functional clock distribution network;  
11                and

12                compensating for the clock of said inter-functional clock distribution  
13                network by inserting said delaying circuit at a terminal of said inter-  
14                function clock distribution network where each of said functional  
15                circuits is connected to said inter-functional clock distribution network.

1     2.     The method of claim 1 wherein compensating for said clock skew of said inter-  
2           functional clock distribution network comprises the steps of:

3                 determining a clock skew factor for one selected functional circuit  
4                 connected to one selected terminal of said inter-functional clock  
5                 distribution network; and

6 adjusting the delaying circuit within said one selected functional circuit to  
7 cancel out said clock skew factor.

1 3. The method of claim 2 wherein said delaying circuit includes:

2 a plurality of delaying buffer circuits, each delaying buffer circuit having an  
3 first increment of delay; and

4 a plurality of interconnecting wiring segments placed between each of the  
5 plurality of delaying buffer circuits, said interconnecting wiring  
6 segments having a second increment of delay.

1 4. The method of claim 3 wherein adjusting said delaying circuit comprises the step  
2 of connecting a first quantity of said delaying buffer circuits with a second  
3 quantity of said plurality of interconnecting wiring segments such that a sum of  
4 the first increment of delay of said first quantity of the delaying buffer circuits and  
5 the second quantity of delay of said interconnecting wiring segments is equal to  
6 the clock skew factor.

1 5. An apparatus for synthesizing a clock distribution circuit within an integrated ✓  
2 circuit device, said device comprised of a plurality of functional circuits and  
3 placed on a substrate, said apparatus comprising:

4 means for allocating at least one delaying circuit within each of said  
5 functional circuits;

6 means for fabricating an intra-functional clock distribution network within  
7 each of the functional circuits;  
8 means for fabricating an inter-functional clock distribution network  
9 between each of the functional circuits;  
10 means for determining a clock skew for the inter-functional clock  
11 distribution network; and  
12 means for compensating for the clock of said inter-functional clock  
13 distribution network by inserting said delaying circuit at a terminal of  
14 said inter-function clock distribution network where each of said  
15 functional circuits is connected to said inter-functional clock distribution  
16 network.

1 6. The apparatus of claim 5 wherein means for compensating for said clock skew of  
2 said inter-functional clock distribution network comprises:

3 means for determining a clock skew factor for one selected functional  
4 circuit connected to one selected terminal of said inter-functional clock  
5 distribution network; and  
6 means for adjusting the delaying circuit within said one selected functional  
7 circuit to cancel out said clock skew factor.

1 7. The apparatus of claim 6 wherein said delaying circuit includes:

2 a plurality of delaying buffer circuits, each delaying buffer circuit having an  
3 first increment of delay; and

4 a plurality of interconnecting wiring segments placed between each of the  
5 plurality of delaying buffer circuits, said interconnecting wiring  
6 segments having a second increment of delay.

1 8. The apparatus of claim 7 wherein the means for adjusting said delaying circuit  
2 comprises means for connecting a first quantity of said delaying buffer circuits  
3 with a second quantity of said plurality of interconnecting wiring segments such  
4 that a sum of the first increment of delay of said first quantity of the delaying  
5 buffer circuits and the second quantity of delay of said interconnecting wiring  
6 segments is equal to the clock skew factor.

1 9. An apparatus for synthesizing a clock distribution circuit within an integrated  
2 circuit device, said device comprised of a plurality of functional circuits and  
3 placed on a substrate, said apparatus comprising means for executing the steps  
4 of:

5 allocating at least one delaying circuit within each of said functional  
6 circuits;

7 fabricating an intra-functional clock distribution network within each of the  
8 functional circuits;

9 fabricating an inter-functional clock distribution network between each of  
10 the functional circuits;  
11 determining a clock skew for the inter-functional clock distribution network;  
12 and  
13 compensating for the clock of said inter-functional clock distribution  
14 network by inserting said delaying circuit at a terminal of said inter-  
15 function clock distribution network where each of said functional  
16 circuits is connected to said inter-functional clock distribution network;

17 10. The apparatus of claim 9 wherein compensating for said clock skew of said inter-  
18 functional clock distribution network comprises the steps of:

19 determining a clock skew factor for one selected functional circuit  
20 connected to one selected terminal of said inter-functional clock  
21 distribution network; and  
22 adjusting the delaying circuit within said one selected functional circuit to  
23 cancel out said clock skew factor.

1 11. The apparatus of claim 10 wherein said delaying circuit includes:

2 a plurality of delaying buffer circuits, each delaying buffer circuit having an  
3 first increment of delay; and

4 a plurality of interconnecting wiring segments placed between each of the  
5 plurality of delaying buffer circuits, said interconnecting wiring  
6 segments having a second increment of delay.

1 12. The apparatus of claim 11 wherein adjusting said delaying circuit comprises the  
2 step of connecting a first quantity of said delaying buffer circuits with a second  
3 quantity of said plurality of interconnecting wiring segments such that a sum of  
4 the first increment of delay of said first quantity of the delaying buffer circuits and  
5 the second quantity of delay of said interconnecting wiring segments is equal to  
6 the clock skew factor.

1 13. A clock distribution circuit within an integrated circuit device, said device  
2 comprised of a plurality of functional circuits and placed on a substrate, said  
3 clock distribution circuit comprising:

4 at least one delaying circuit placed within each of said functional circuits;

5 an intra-functional clock distribution network within each of the functional  
6 circuits; and

7 an inter-functional clock distribution network between each of the  
8 functional circuits;

9 wherein a clock skew for the inter-functional clock distribution network is  
10 compensated by inserting said delaying circuit at a terminal of said

11 inter-function clock distribution network where each of said functional  
12 circuits is connected to said inter-functional clock distribution network.

1 14. The clock distribution circuit of claim 12 wherein compensating for said clock  
2 skew of said inter-functional clock distribution network comprises the steps of:

3 determining a clock skew factor for one selected functional circuit

4 connected to one selected terminal of said inter-functional clock  
5 distribution network; and

6 adjusting the delaying circuit within said one selected functional circuit to  
7 cancel out said clock skew factor.

1 15. The clock distribution circuit of claim 14 wherein said delaying circuit includes:

2 a plurality of delaying buffer circuits, each delaying buffer circuit having an  
3 first increment of delay; and

4 a plurality of interconnecting wiring segments placed between each of the  
5 plurality of delaying buffer circuits, said interconnecting wiring  
6 segments having a second increment of delay.

1 16. The clock distribution circuit of claim 3 wherein adjusting said delaying circuit  
2 comprises the step of connecting a first quantity of said delaying buffer circuits  
3 with a second quantity of said plurality of interconnecting wiring segments such  
4 that a sum of the first increment of delay of said first quantity of the delaying

5           buffer circuits and the second quantity of delay of said interconnecting wiring  
6           segments is equal to the clock skew factor.

1   17.   A integrated circuit synthesizing apparatus for synthesizing an integrated circuit  
2           device, said device comprised of a plurality of functional circuits and placed on a  
3           substrate, said integrated circuit synthesizing apparatus executing the steps of:

4                   synthesizing a clock distribution circuit within said integrated circuit device,  
5                   said synthesizing comprising the steps of:

6                           allocating at least one delaying circuit within each of said functional  
7                           circuits;

8                           fabricating an intra-functional clock distribution network within each of  
9                           the functional circuits;

10                          fabricating an inter-functional clock distribution network between each  
11                          of the functional circuits;

12                          determining a clock skew for the inter-functional clock distribution  
13                          network; and

14                          compensating for the clock of said inter-functional clock distribution  
15                          network by inserting said delaying circuit at a terminal of said inter-  
16                          function clock distribution network where each of said functional  
17                          circuits is connected to said inter-functional clock distribution  
18                          network;



1 18. The integrated circuit synthesizing apparatus of claim 17 wherein compensating  
2 for said clock skew of said inter-functional clock distribution network comprises  
3 the steps of:

4 determining a clock skew factor for one selected functional circuit

5 connected to one selected terminal of said inter-functional clock

6 distribution network; and

7 adjusting the delaying circuit within said one selected functional circuit to

8 cancel out said clock skew factor.

1 19. The integrated circuit synthesizing apparatus of claim 18 wherein said delaying  
2 circuit includes:

3 a plurality of delaying buffer circuits, each delaying buffer circuit having an

4 first increment of delay; and

5 a plurality of interconnecting wiring segments placed between each of the

6 plurality of delaying buffer circuits, said interconnecting wiring

7 segments having a second increment of delay.

1 20. The integrated circuit synthesizing apparatus of claim 19 wherein adjusting said  
2 delaying circuit comprises the step of connecting a first quantity of said delaying  
3 buffer circuits with a second quantity of said plurality of interconnecting wiring  
4 segments such that a sum of the first increment of delay of said first quantity of

5 the delaying buffer circuits and the second quantity of delay of said  
6 interconnecting wiring segments is equal to the clock skew factor.

1 21. A medium for retaining a computer program which, when executed on a 6  
2 computing system, executes a process for synthesizing a clock distribution circuit  
3 within an integrated circuit device, said device comprised of a plurality of  
4 functional circuits and placed on a substrate, said process comprising the steps  
5 of:

6 allocating at least one delaying circuit within each of said functional  
7 circuits;

8 fabricating an intra-functional clock distribution network within each of the  
9 functional circuits;

10 fabricating an inter-functional clock distribution network between each of  
11 the functional circuits;

12 determining a clock skew for the inter-functional clock distribution network;  
13 and

14 compensating for the clock of said inter-functional clock distribution  
15 network by inserting said delaying circuit at a terminal of said inter-  
16 function clock distribution network where each of said functional  
17 circuits is connected to said inter-functional clock distribution network.

1   22.   The medium of claim 20 wherein compensating for said clock skew of said inter-  
2       functional clock distribution network comprises the steps of:

3               determining a clock skew factor for one selected functional circuit  
4               connected to one selected terminal of said inter-functional clock  
5               distribution network; and

6               adjusting the delaying circuit within said one selected functional circuit to  
7               cancel out said clock skew factor.

1   23.   The medium of claim 21 wherein said delaying circuit includes:

2               a plurality of delaying buffer circuits, each delaying buffer circuit having an  
3               first increment of delay; and

4               a plurality of interconnecting wiring segments placed between each of the  
5               plurality of delaying buffer circuits, said interconnecting wiring  
6               segments having a second increment of delay.

1   24.   The medium of claim 22 wherein adjusting said delaying circuit comprises the  
2       step of connecting a first quantity of said delaying buffer circuits with a second  
3       quantity of said plurality of interconnecting wiring segments such that a sum of  
4       the first increment of delay of said first quantity of the delaying buffer circuits and  
5       the second quantity of delay of said interconnecting wiring segments is equal to  
6       the clock skew factor.